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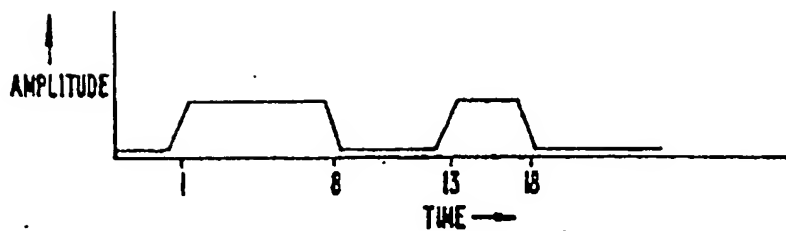


FIG. 1A (BACKGROUND)

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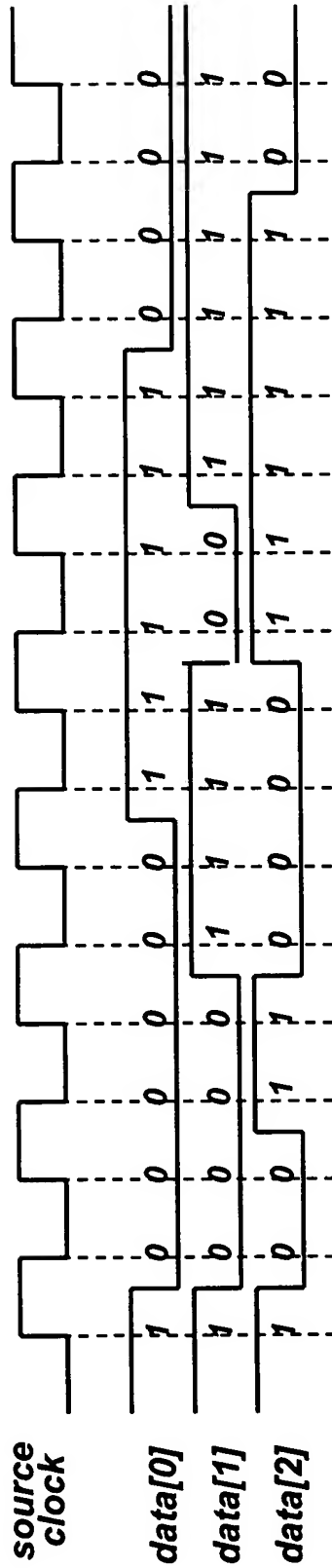


Fig. 1B (Background) Source Synchronous Data Bus

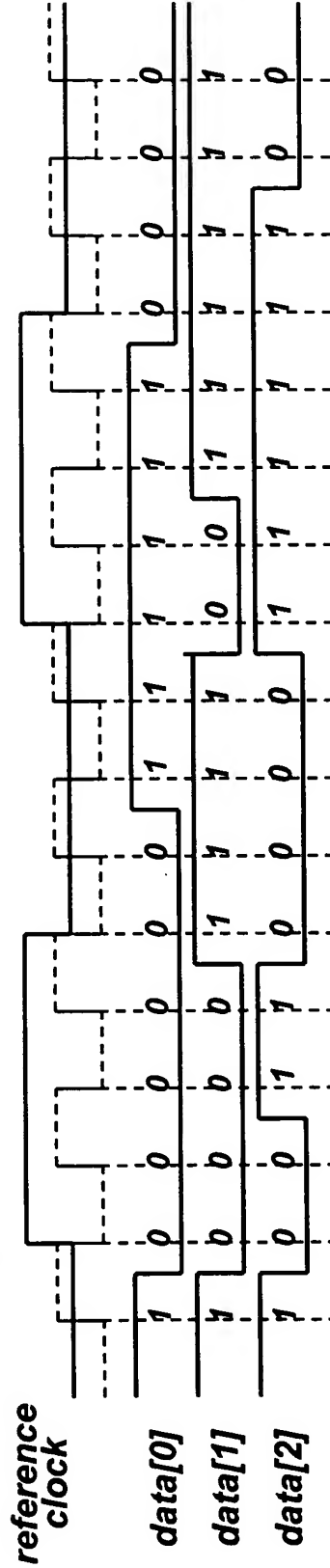
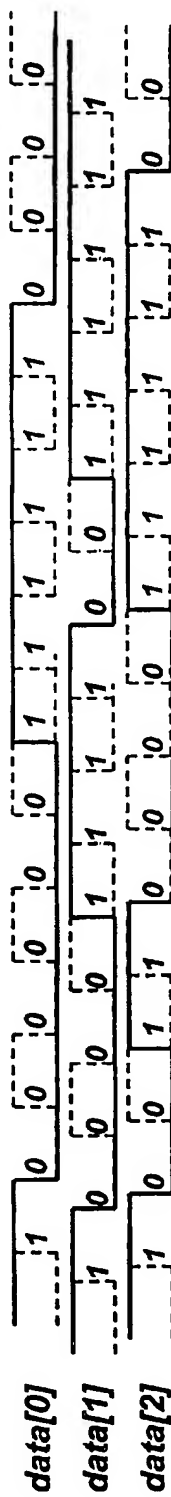


Fig. 1C (Background) Reference Clock Synchronous Data Bus



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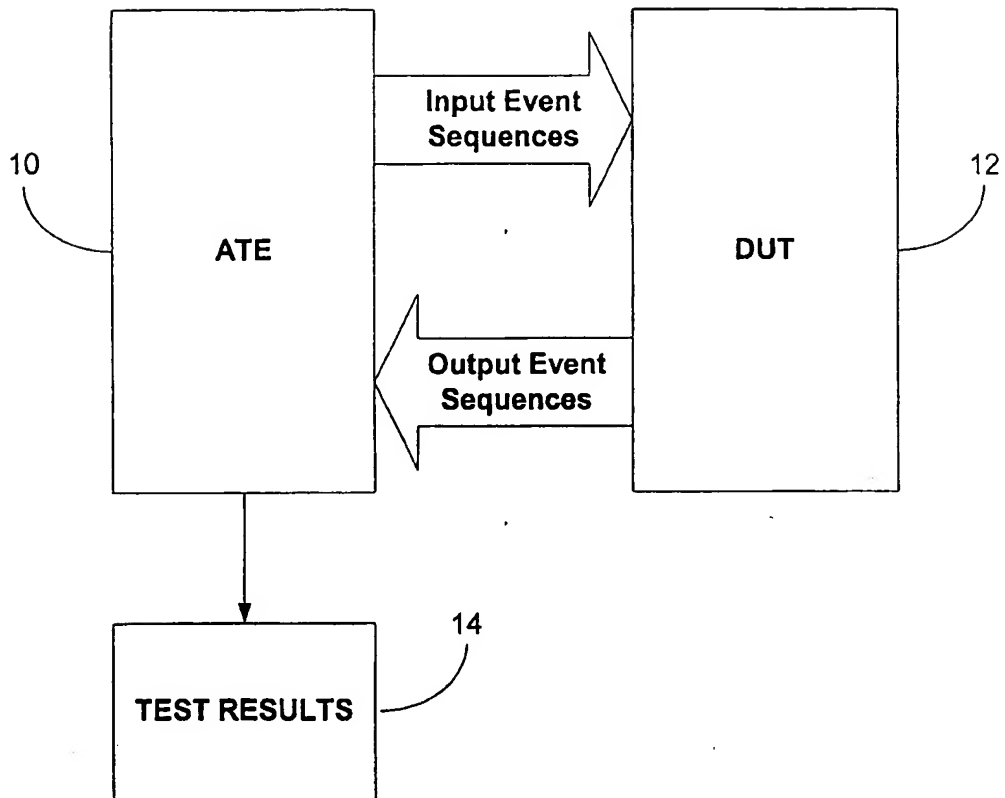


Figure 2

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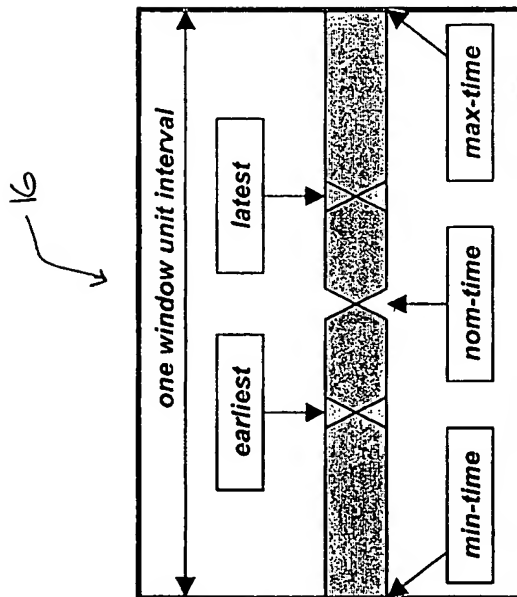


Figure 3

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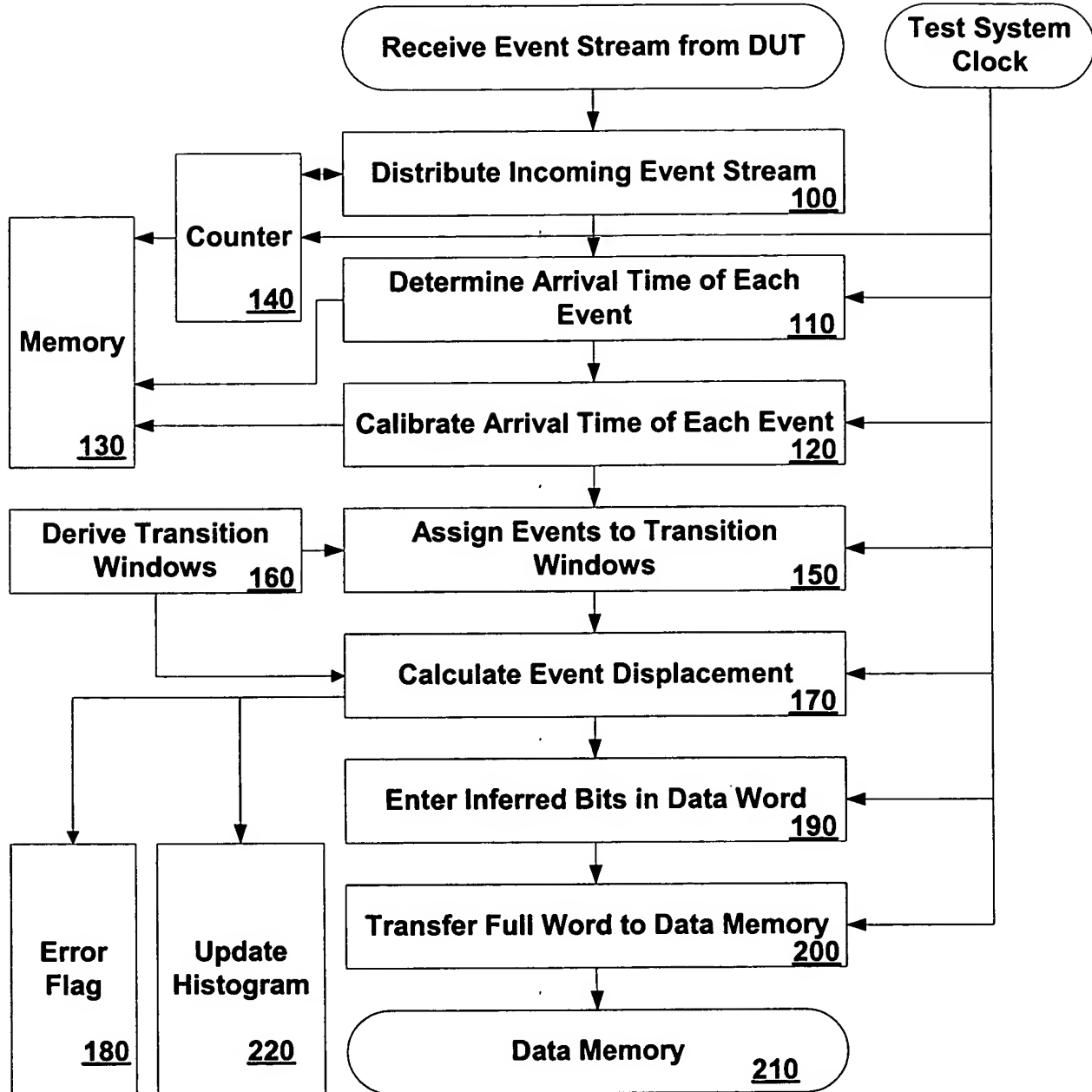


Figure 4

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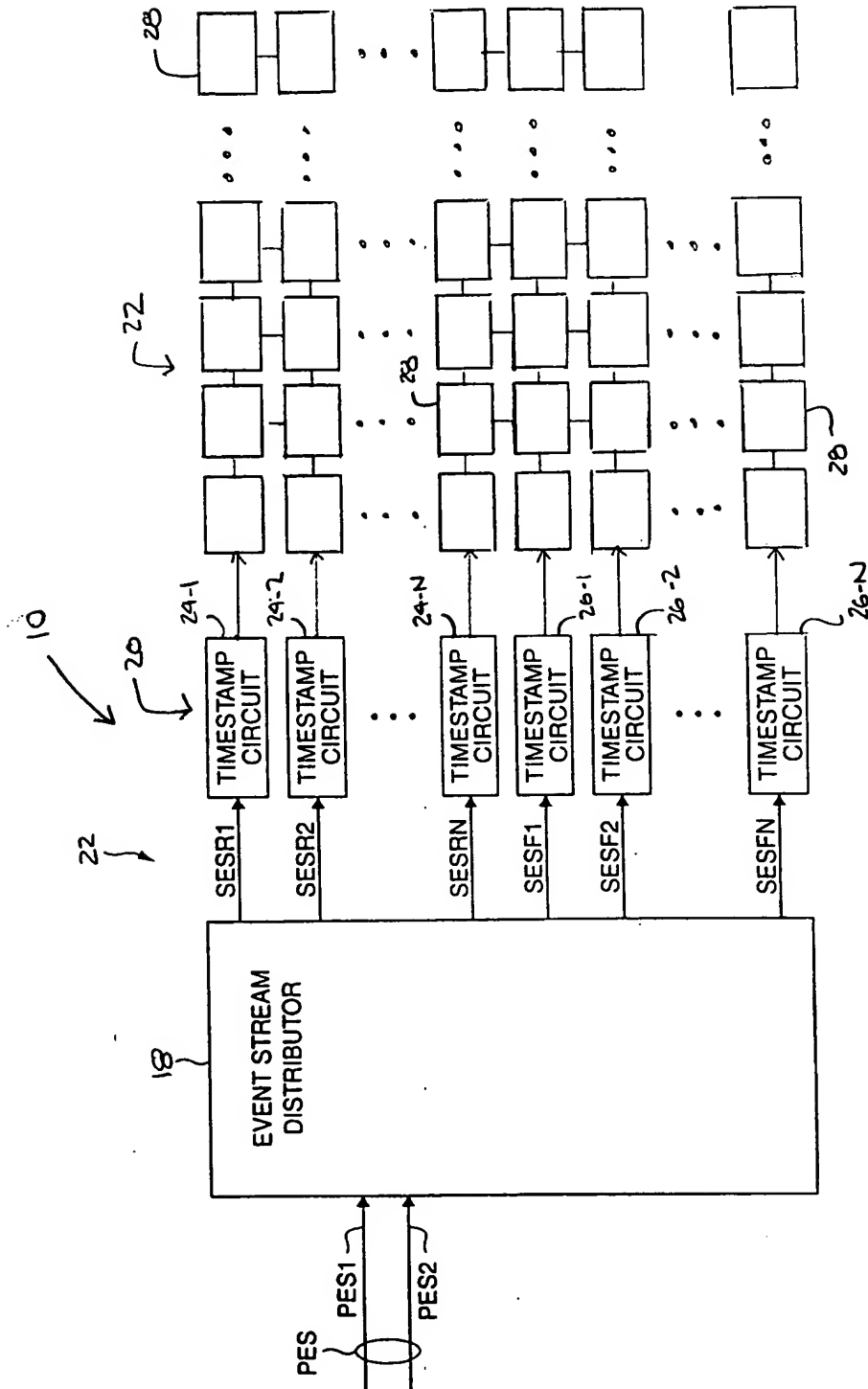


FIG. 5

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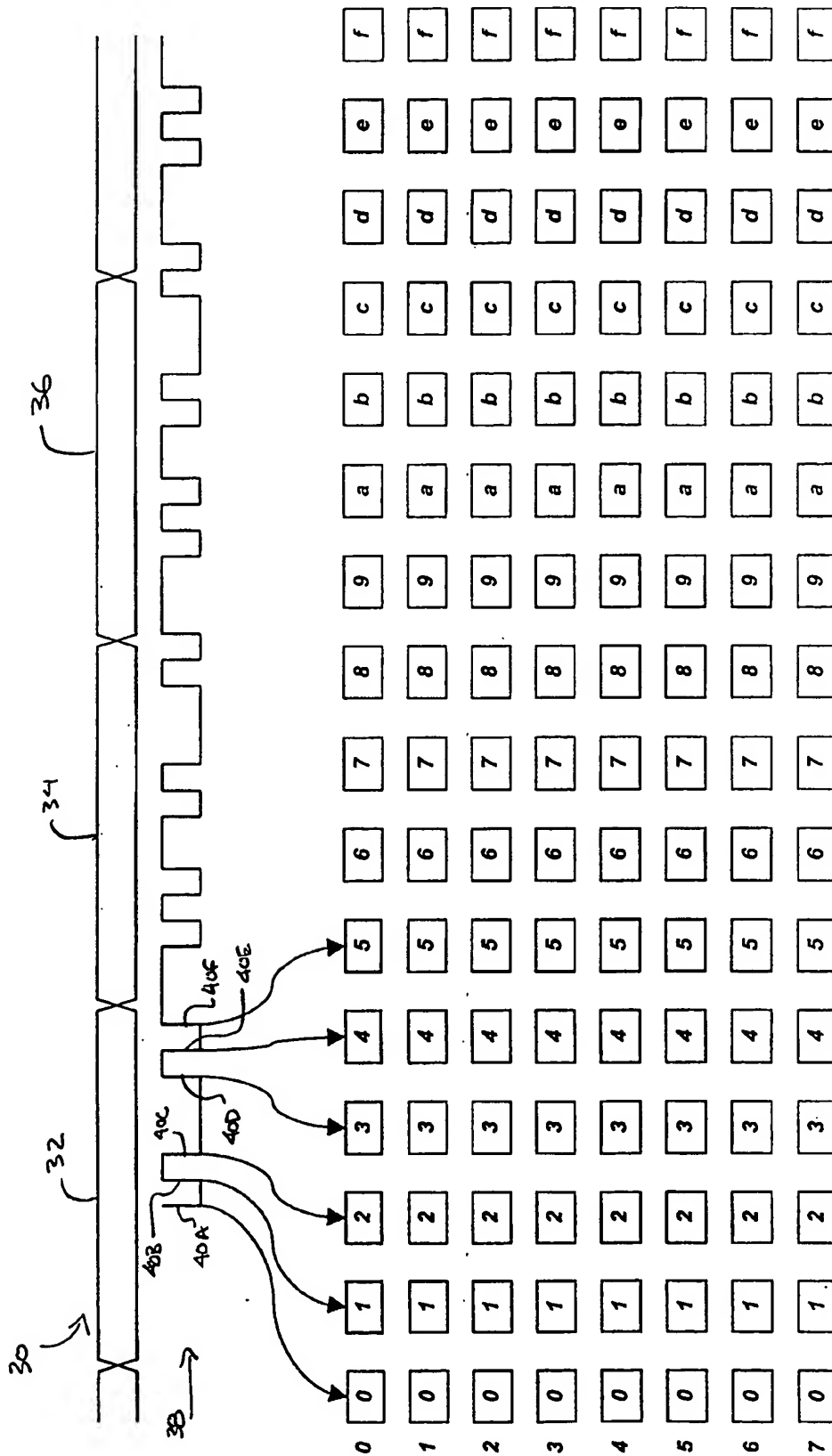


Figure 6A

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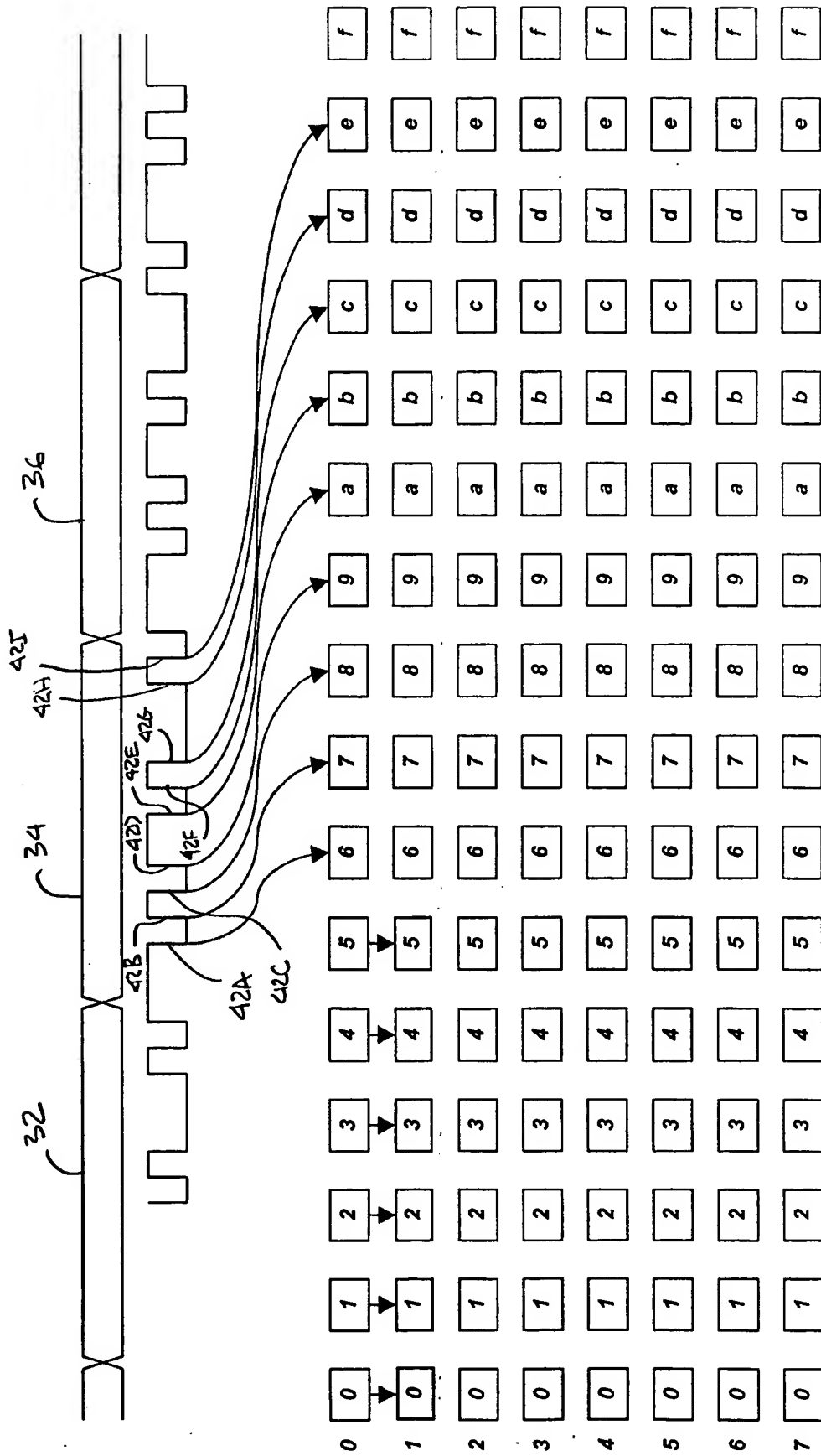
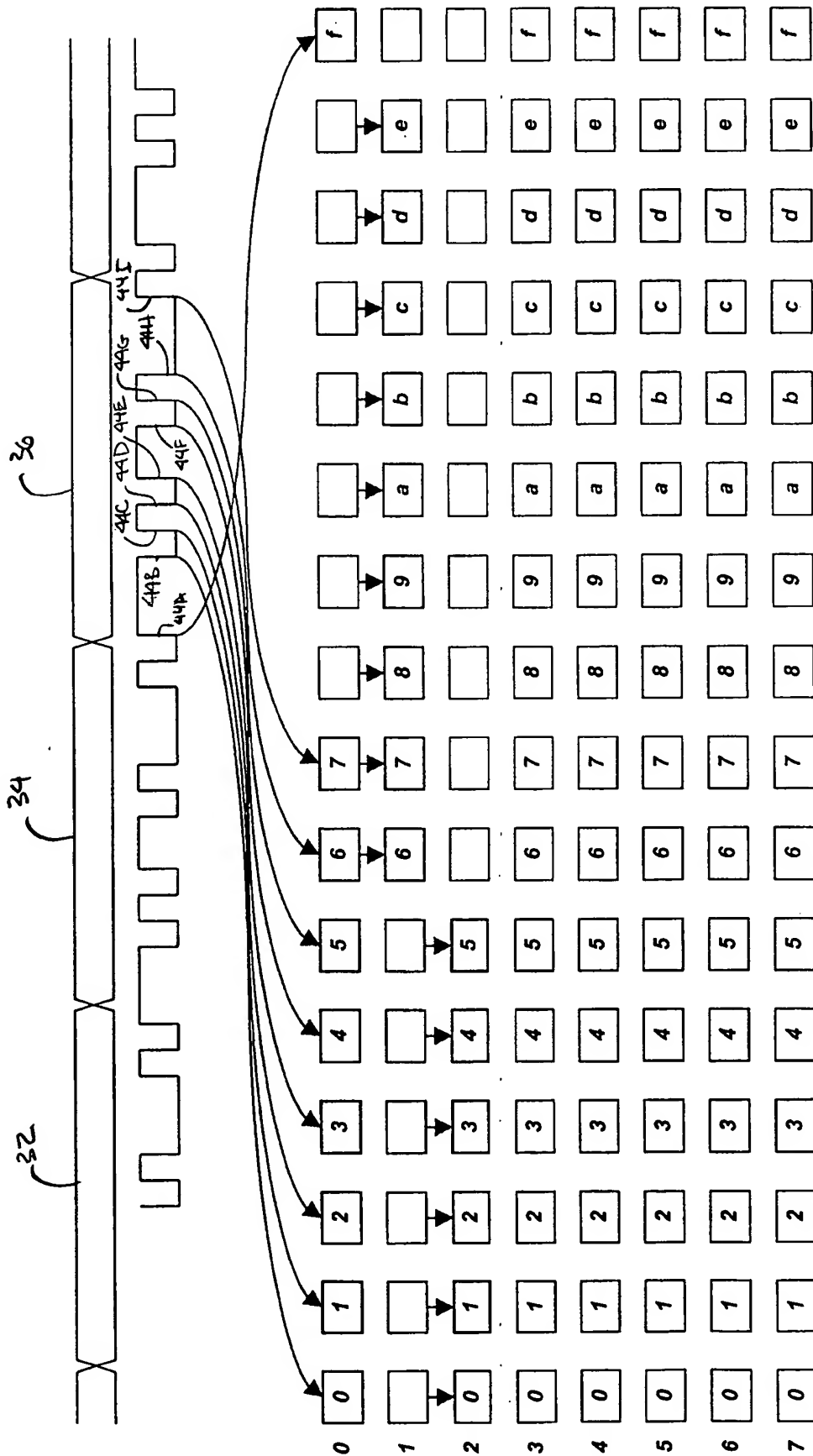
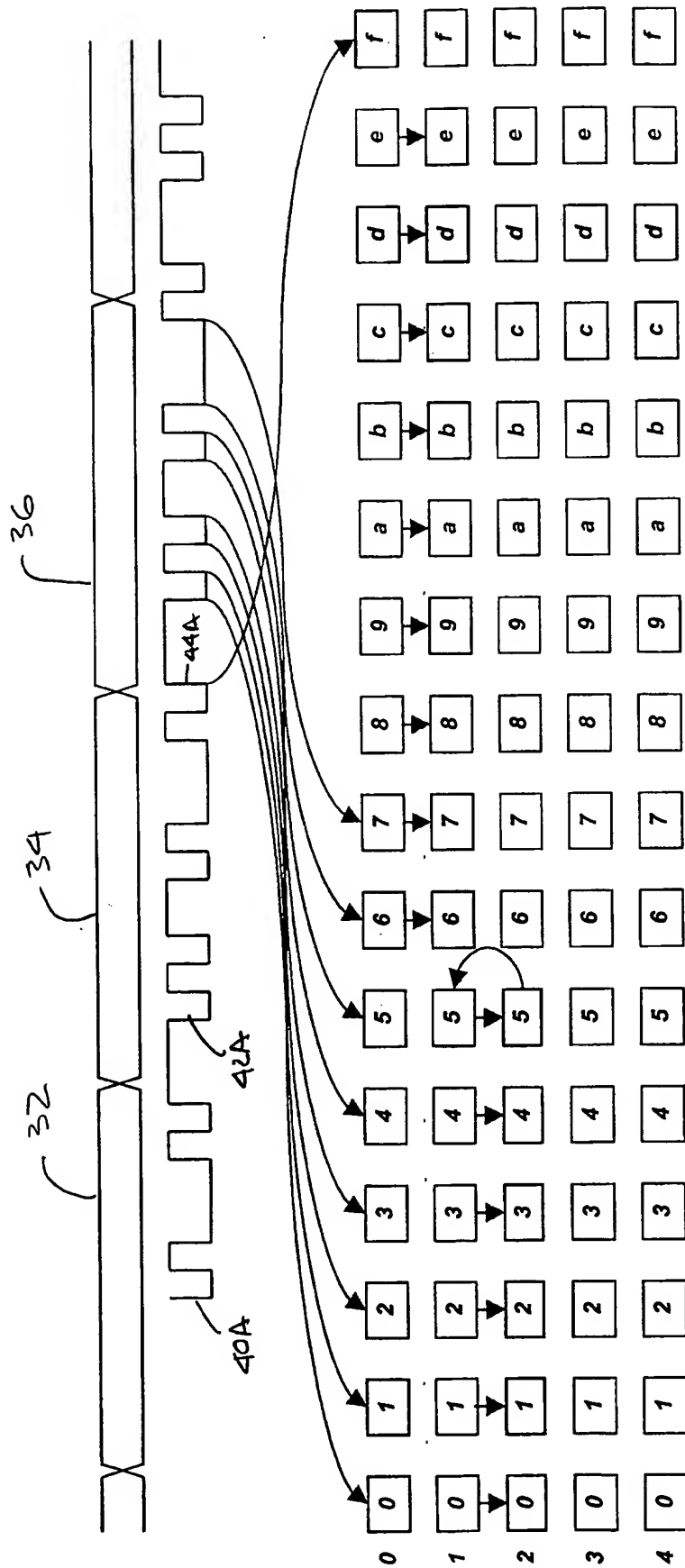


Figure 6B



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Figure 6C



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Figure 6D

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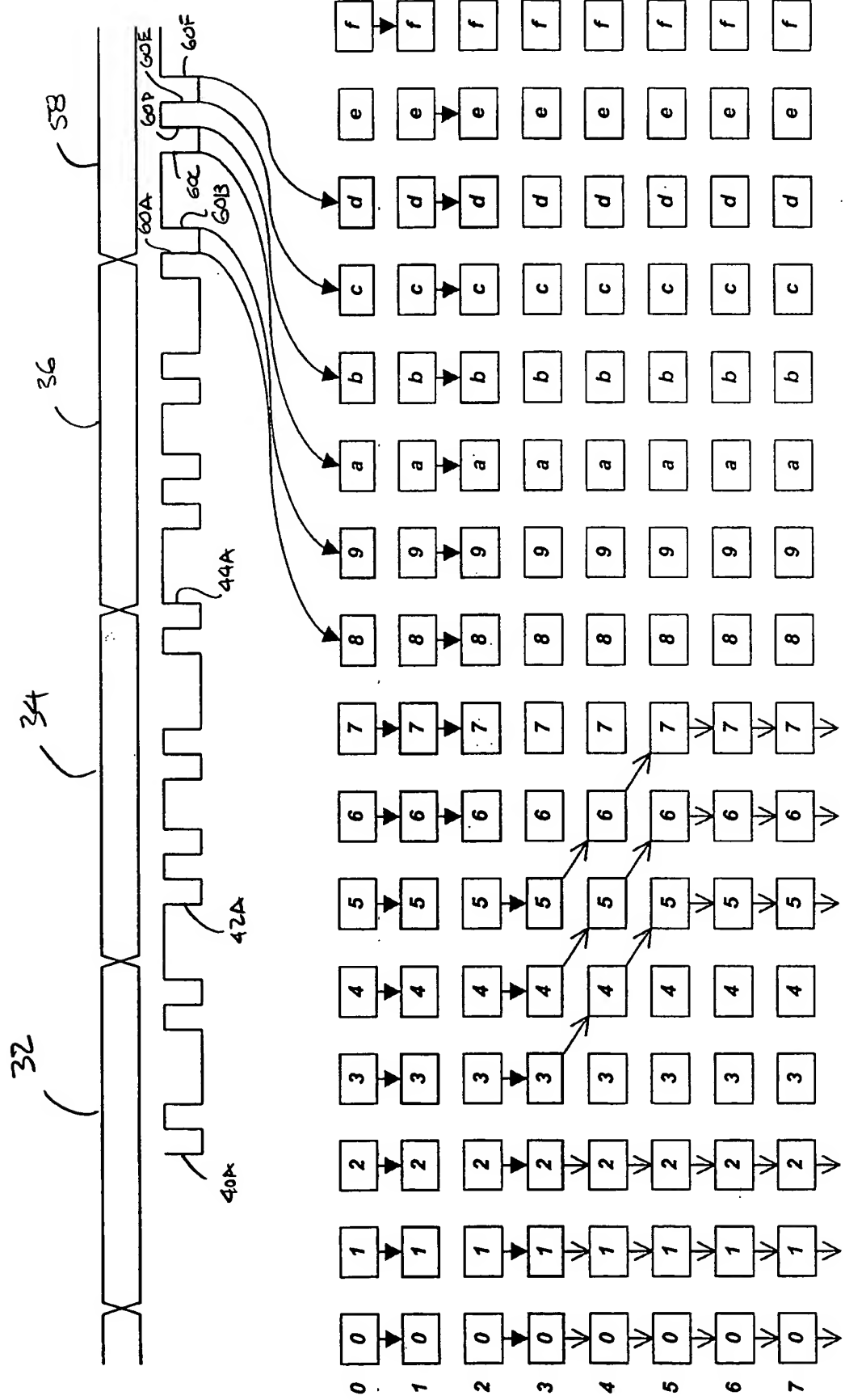


Figure 6E



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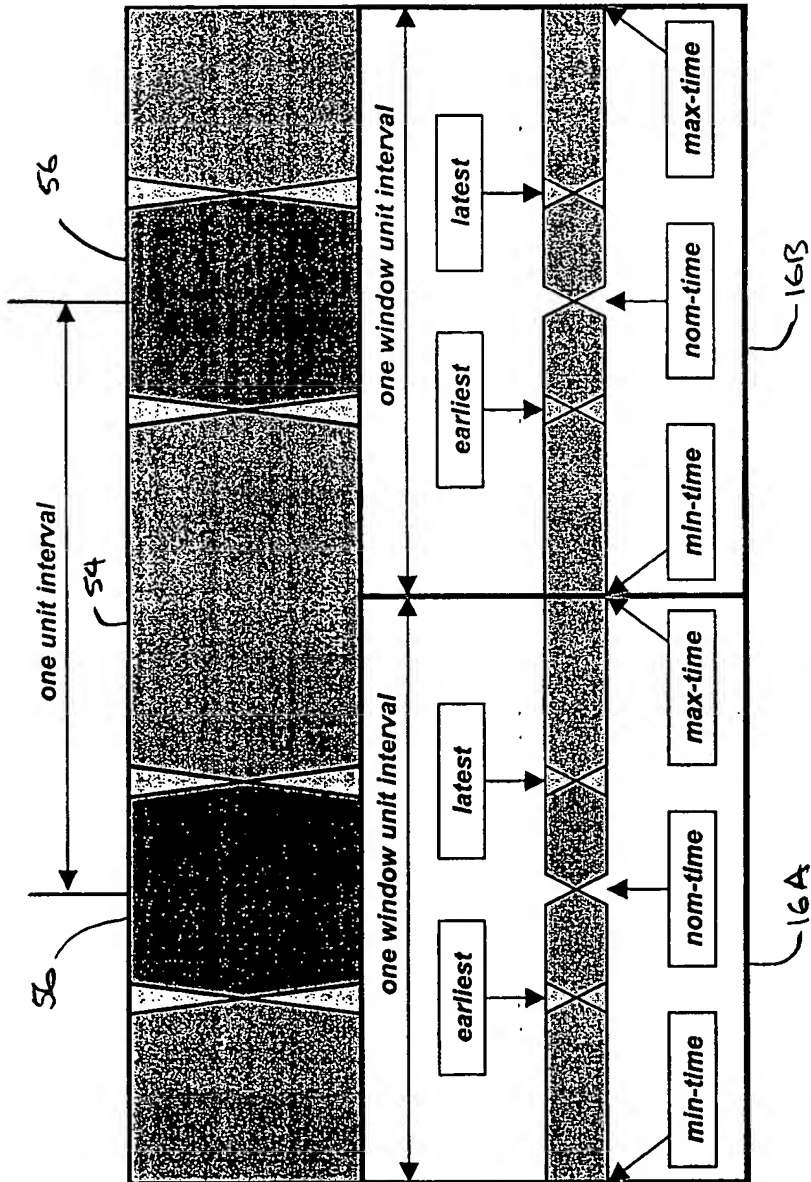


Figure 8

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Change colored cells for operation		Channel Offset	Clock cycle after enable	Channel 0						Channel 1					
				Min	Nom	Max	Earliest	Latest	Min	Nom	Max	Earliest	Latest		
Period(ps)	2500	32	0	0	32	63	24	40	64	96	127	88	104		
Resolution	256		1	128	160	191	152	168	192	224	255	216	232		
LSB(ps)	9.766		2	0	32	63	24	40	64	96	127	88	104		
Rate(GBPS)	1.6		3	128	160	191	152	168	192	224	255	216	232		
Margin	12.5%		4	0	32	63	24	40	64	96	127	88	104		
UI NOM(LSB)	64		5	128	160	191	152	168	192	224	255	216	232		
			6	0	32	63	24	40	64	96	127	88	104		
			7	128	160	191	152	168	192	224	255	216	232		
			8	0	32	63	24	40	64	96	127	88	104		
			9	128	160	191	152	168	192	224	255	216	232		
			10	0	32	63	24	40	64	96	127	88	104		
			11	128	160	191	152	168	192	224	255	216	232		
			12	0	32	63	24	40	64	96	127	88	104		
			13	128	160	191	152	168	192	224	255	216	232		
			14	0	32	63	24	40	64	96	127	88	104		
			15	128	160	191	152	168	192	224	255	216	232		
			16	0	32	63	24	40	64	96	127	88	104		
			17	128	160	191	152	168	192	224	255	216	232		
			18	0	32	63	24	40	64	96	127	88	104		
			19	128	160	191	152	168	192	224	255	216	232		
			20	0	32	63	24	40	64	96	127	88	104		
			21	128	160	191	152	168	192	224	255	216	232		
			22	0	32	63	24	40	64	96	127	88	104		
			23	128	160	191	152	168	192	224	255	216	232		
			24	0	32	63	24	40	64	96	127	88	104		

FIG. 9A

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expressed in LSB - TimeStamper ATE

clock cycle after enable	Channel					Channel					Channel				
	Min	Nom	Max	Earliest	Latest	Min	Nom	Max	Earliest	Latest	Min	Nom	Max	Earliest	Latest
0	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
1	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
2	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
3	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
4	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
5	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
6	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
7	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
8	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
9	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
10	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
11	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
12	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
13	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
14	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
15	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
16	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
17	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
18	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
19	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
20	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
21	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
22	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
23	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
24	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40

FIG. 9B

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clock cycle after enable	Channel					Channel					Channel				
	Min	Nom	Max	Earliest	Latest	Min	Nom	Max	Earliest	Latest	Min	Nom	Max	Earliest	Latest
0	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
1	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
2	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
3	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
4	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
5	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
6	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
7	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
8	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
9	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
10	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
11	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
12	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
13	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
14	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
15	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
16	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
17	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
18	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
19	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
20	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
21	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
22	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
23	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
24	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232

Pg. 9C

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clock cycle after enable	Channel					Channel					Channel				
	Min	Nom	Max	Earliest	Latest	Min	Nom	Max	Earliest	Latest	Min	Nom	Max	Earliest	Latest
0	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
1	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
2	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
3	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
4	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
5	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
6	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
7	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
8	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
9	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
10	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
11	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
12	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
13	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
14	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
15	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
16	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
17	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
18	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
19	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
20	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
21	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
22	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
23	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
24	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168

Fig. 9D

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clock cycle after enable	Channel					Channel					Channel				
	Min	Nom	Max	Earliest	Latest	Min	Nom	Max	Earliest	Latest	Min	Nom	Max	Earliest	Latest
0	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
1	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
2	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
3	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
4	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
5	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
6	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
7	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
8	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
9	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
10	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
11	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
12	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
13	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
14	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
15	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
16	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
17	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
18	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
19	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
20	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
21	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
22	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
23	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
24	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104

FIG. 9 E

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clock cycle after enable	Channel 14					Channel 15					Channel 16				
	Min	Nom	Max	Earliest	Latest	Min	Nom	Max	Earliest	Latest	Min	Nom	Max	Earliest	Latest
0	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
1	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
2	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
3	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
4	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
5	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
6	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
7	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
8	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
9	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
10	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
11	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
12	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
13	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
14	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
15	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
16	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
17	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
18	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
19	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
20	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
21	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
22	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40
23	0	32	63	24	40	64	96	127	88	104	128	160	191	152	168
24	128	160	191	152	168	192	224	255	216	232	0	32	63	24	40

Fig. 9F

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clock cycle after enable	Channel					Channel					Channel				
	Min	Nom	Max	Earliest	Latest	Min	Nom	Max	Earliest	Latest	Min	Nom	Max	Earliest	Latest
0	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
1	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
2	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
3	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
4	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
5	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
6	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
7	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
8	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
9	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
10	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
11	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
12	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
13	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
14	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
15	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
16	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
17	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
18	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
19	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
20	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
21	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
22	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232
23	192	224	255	216	232	0	32	63	24	40	64	96	127	88	104
24	64	96	127	88	104	128	160	191	152	168	192	224	255	216	232

FIG. 9G

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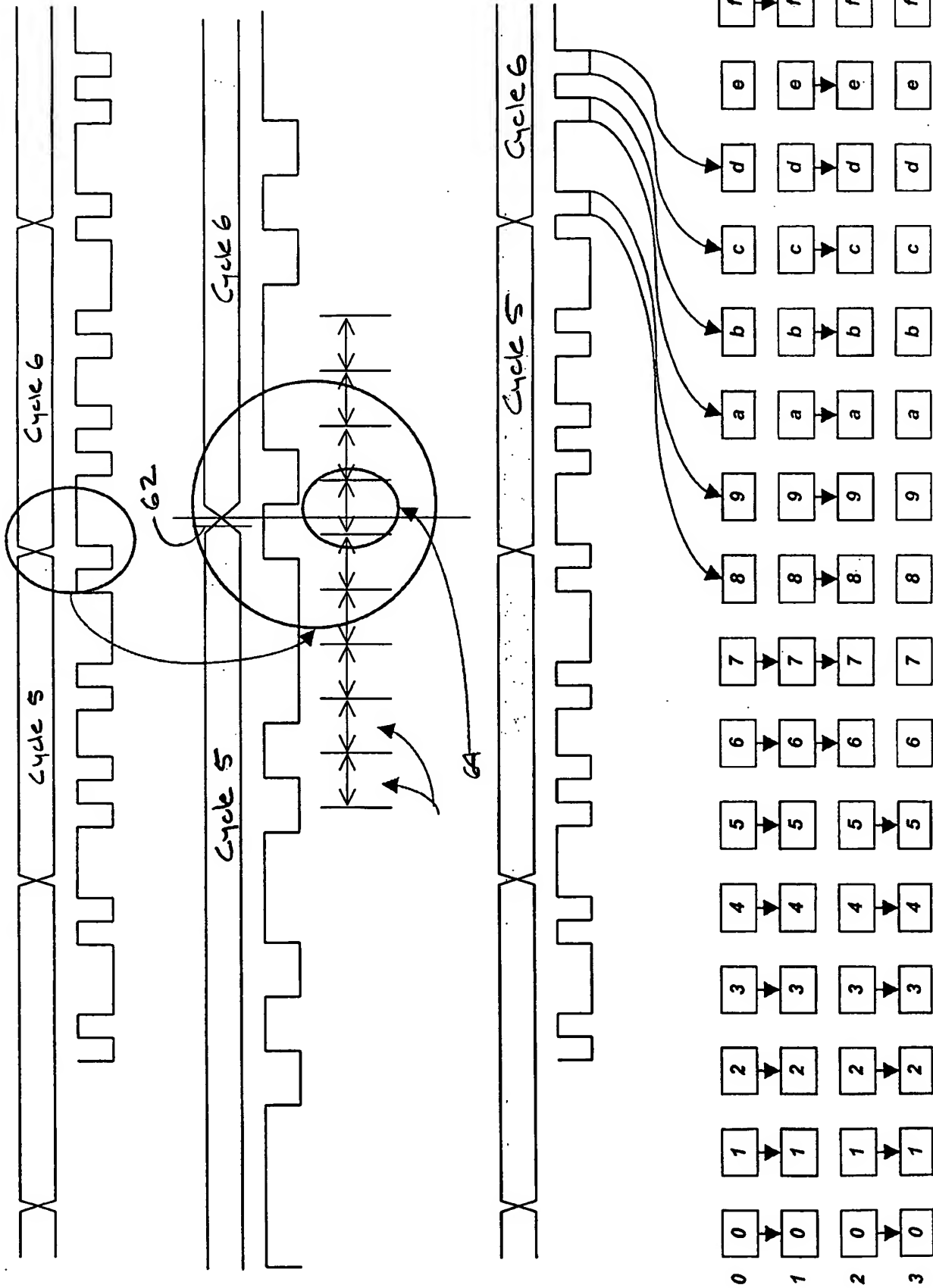


Figure 10

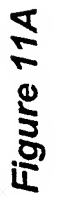


Figure 11A

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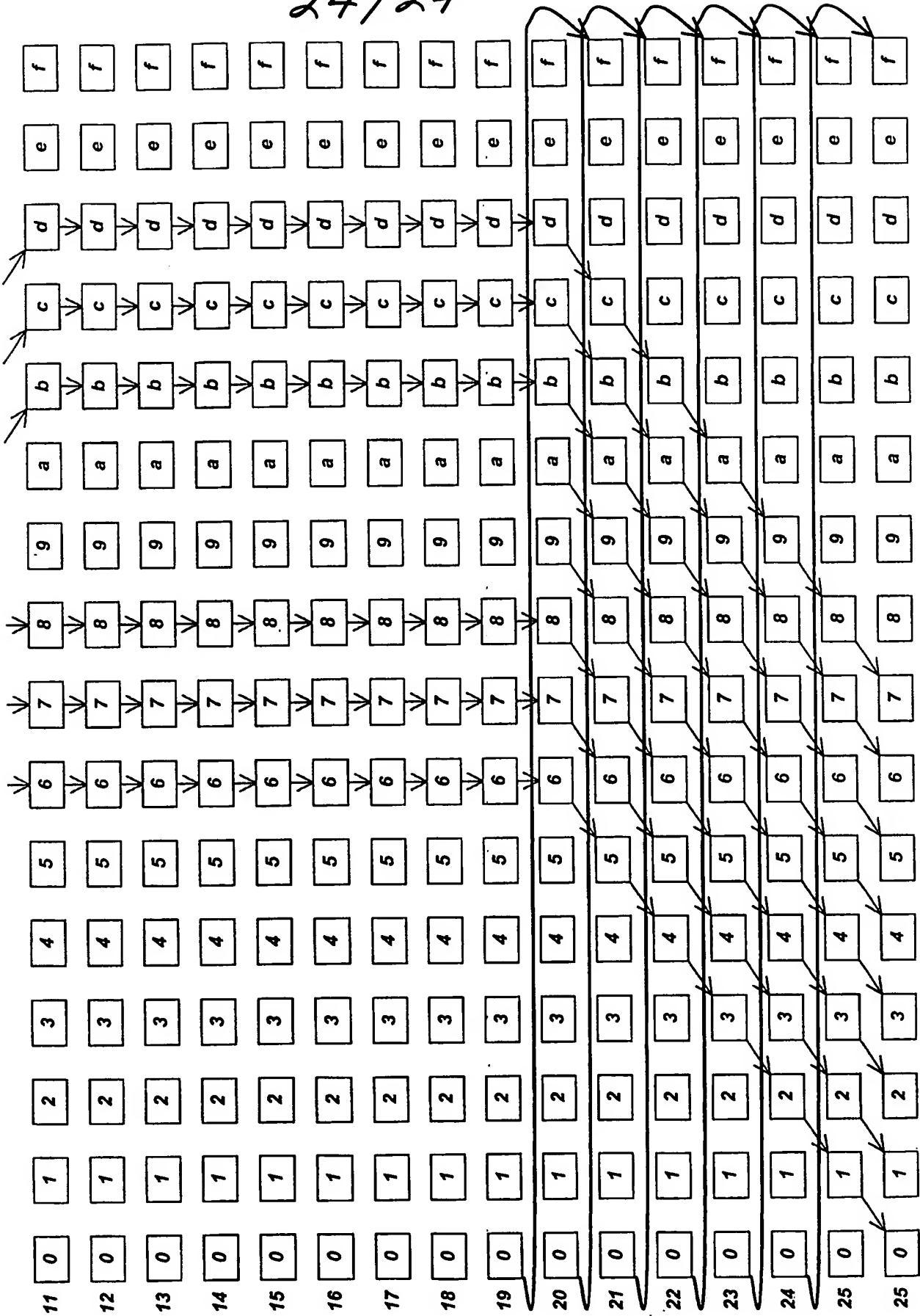


Figure 11B